REMARKS

Claims 17–35 are pending in the present application.

Claim 16 was canceled herein, and claims 20, 23–24, 26 and 28–35 were amended.

Claims 17–19 are allowed.

Claims 26, 31 and 32 are objected to.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 102 (Anticipation)

Claims 20–21 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,903,312 to *Malladi et.* This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-73 (8th ed. rev. 2 May 2004).

Independent claim 20 has been amended to substantially conform in scope to claim 1 in the parent application, serial no. 09/207,343 (now U.S. Patent No. 6,414,996). As with allowed independent claim 1 in the parent application, independent claim 20 recites a controller that executes instructions driving the motion compensation for the video processor. This allows the calculation of memory addresses and generation of pipeline control information to proceed in parallel with the data manipulation. As noted in the parent application, such a feature is not found in *Malladi et al.* *Malladi et al* describes a reference memory controller 402 and associated control register 410:

Motion compensation unit 176 includes a motion compensation pipeline which includes a reference memory controller 402 which receives input pixel values, a half pel compensation block 404, a B-picture compensation unit 406, and a compensation macroblock RAM 408. Motion compensated pixel values stored in RAM 408 are periodically provided to merge and store unit 174 through an interface 426.

The inputs to reference memory controller 402 include a group of four pixel values of one byte each provided on data path 414 (mcref__[31:0]). This data includes four bytes, one byte for each of four adjacent locations on a row of luminance or chrominance values. Other data to reference memory controller 402 is provided to as a one byte value which will be provided only when right half pel averaging is being performed and only when the right-most group of five values are to be half pel average. In other words, this data path is reserved for the right-most pixel value in data that is to be right half pel average. This single byte of data is provided on data path 416 (mcref__[7:0]). Other inputs to reference memory controller 402 include a one bit signal 418 (mc__word__en) which, when set high, indicates that motion compensation data is on line 414. Finally, a one bit input signal 420 (mc__byte__en) indicates, when set high, that valid data is on line 416.

The reference memory controller 402 includes the necessary handshaking logic to take in data. It also includes logic for determining if right half pet compensation is necessary and routing the appropriate values over 32-bit line 403 and 8-bit line 405. Normally, groups of four adjacent pixel values are routed over line 403. However, when right half pel averaging is to be performed and the right-most collection of 5 input bytes is to be processed, the right-most pixel value is sent over line 405. Reference memory controller 402 will know when to expect right half pel compensation values based upon information from the appropriate decoded motion vector, which information is stored in a control register within a group of control registers 410. If no half pel compensation is necessary, reference memory controller 402 simply directs the input pixel values to be stored in compensation macrobyte RAM 408, without processing in either half pel compensation unit 404 or B-picture compensation unit 406.

. . . .

Control register 410 provides the information to allow the motion compensation unit 176 to perform the appropriate operations depending upon the current clock cycle. From such information it is known which four or five pixel values are being input to controller 402. It also provides the system with knowledge of whether forward or backward motion references are employed. Further, it provides information to whether a first or second vector (associated with two different fields) are being processed. Output 422 (mc__ref__status) from control registers 410

> indicates whether the motion compensation pipeline is active and the status of the compensation macroblock RAM 408. This information is important, as no additional input data can be provided to controller 402 until RAM 408 is available for fresh pixel values. A register interface 424 is provided between the control registers 410 and the larger bank of registers 164 shown in FIG. 2.

Malladi et al, column 27, line 43 through column 28, line 18, column 29, lines 5–21. Thus, *Malladi* does not disclose a controller executing instructions to provide motion compensation during video decoding. Neither reference memory controller 402 nor control register 410 execute instructions at all. Reference memory controller 402 merely stores pixel values directly or forwards them to other units depending on whether half pel or B-picture compensation is necessary, while control register 410 appears to do nothing more than store configuration data used by other components.

Therefore, the rejection of claims 20–21 under 35 U.S.C. § 102 has been overcome.

35 U.S.C. § 103 (Obviousness)

Claim 22 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Malladi et al.* Claims 23–25 and 27–28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over "Admitted Prior Art" in view of *Malladi et al.* These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-128 (8th ed. rev. 2 May 2004). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

As with independent claim 20, independent claim 23 has been amended to substantially conform in scope to allowed independent claim 1 from the parent application. As noted both in the parent application and above, the claim includes limitations not found in *Malladi et al.*

Therefore, the rejection of claims 22–25 and 27–28 under 35 U.S.C. § 103 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: 12-29-04

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